Remark

Applicants respectfully request reconsideration of this application as amended. Claims 1, 2, 3, 5, 8, 9, 10, 12 and 17 are amended. No claims have been canceled. No claims have been added. Therefore claims 1-20 are present for examination.

Conclusion

Applicants respectfully submit that the claims as amended are now in condition for allowance. Accordingly, Applicants respectfully request the rejections be withdrawn and the claims as amended be allowed.

Respectfully submitted,

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Version with Markings to Show Changes Made

Insertions are underlined, deletions are stricken.

In the Specification:

Please delete paragraph 13 as filed, and replace with the following paragraph:

[0013] The PCS data path can be considered as having a tx (transmit) path from the XGXS to the PMA and a rx (receive) path from the PMA to the XGXS. As shown in Figure 2, in a tx-path, the PCS interface receives a data stream 69 in XGMII (10 Gigabit Media Independent Interface) format. This format has four eight-bit lanes with each bit double clocked to achieve a ~~312~~ 312.5 Mbit/s data rate on 156.25 MHz lines. The data lanes can be consolidated and then can be divided into pairs of single data rate lines, as shown. The single data rate lines can also be divided up into several slower clock rate lines, as is well-known in the art. The idles removal block 73 analyses the data stream and removes idles, if it is requested to do so by the clock adaptation block 75. It then writes the data with or without idles into a FIFO buffer 77. While removing idles, all input into the FIFO buffer in the clock adaptation block is disabled. An idles insertion block 79 analyses the data stream that it reads from the FIFO buffer 77 and inserts idles, if requested to do so by the clock adaptation block.

Please delete paragraph 20 as filed, and replace with the following paragraph:

[0020] The address range of the DPRAM in this example is divided into eight sections or banks 109. However, any number of banks can be used depending on the application. The number of banks can be selected to be sufficient to compensate for clock rate discrepancies. A set of read/write control signals, two for each of the eight sections,

is accessed by the write control block and read control block to determine access to each of the eight sections, respectively. In the present example shown in Figure 3, the signals are connected across the clock domain 76 by a set of eight banks 107, this provides ~~sixteen~~ 16 synchronization units, two for each bank. When a write cycle has filled the first bank completely, the first read/write control signal is set. The write block continues by filling the following banks. The read block has access to bank 1 after the bank is written, and the signal is set as full. The signal is set as empty when all data of this bank has been read. Both control processes have to set the status signals early enough to allow for signal synchronization between the two different clock domains. If a read bank and a write bank-access occur at the same bank at substantially the same time, then an error 110 can occur. This can be indicated to a 2:1 multiplexer 104 on an error line 110 from the read control block. When an error is indicated /LF/ (local fault words) are inserted from an /LF/ source 106. The local fault words are defined in the 10Gb Ethernet standard. For other applications, other types of error signaling can be used. The generation of overflow and underflow warning signals are described below.

Please delete paragraph 23 as filed, and replace with the following paragraph:

[0023] The underflow and overflow signals are based on the rules for inserting and removing idles, the size of the data packets, the capacity for inserting and removing idles and the speed and latency of the circuitry. With a possible maximum clock speed difference of +/- 200ppm, the 156.25 MHz clocks may differ by as much as 31.25 KHz. Typically, idles cannot be inserted into a data packet but only before or after a packet. In a typical 10 Gb Ethernet application as described in the proposed draft IEEE standard

802.3ae, data packets are from 64 to 1518 octets wide. ~~16~~ 8 octets are transmitted for each clock cycle (at 156.25 MHz SDR). With a maximum clock skew, the system must store at least two packets or from 8 to 190 clocks of data on the write side to avoid errors before idles can be removed. The overflow warning threshold is set so that idles can be removed in time to compensate the discrepancy. Similarly the underflow warning threshold is set so that idles can be inserted in time to compensate the discrepancy. The error signal is set at a higher threshold than the warning signals. This allows an overflow or underflow to be corrected before an error occurs. For other applications, the sizes of the various buffers can be adapted to accommodate the rules for idles in the particular application.

Please delete paragraph 24 as filed, and replace with the following paragraph:

[0024] For a rx path, the PCS module operates in the same way as shown in Figure 2, but in the opposite direction. The PCS module is accordingly reconfigured as shown in Figure 4. The PCS module receives data 87 from the PMA sublayer of the physical layer. This is shown, as above, as two blocks at a 156.25 MHz single data rate, however other configurations are also possible. These are processed by the other modules 115 as desired for the particular application. In 10Gb Ethernet, the other modules include descrambling, decoding, data rate conversion, and packet reconfiguration. For other applications other modules may be provided. The data blocks are received by an idle removal block 117. Idles are removed or inserted from the data in the idle removal 117 and insertion 119 blocks, as requested by the clock adaptation block 121. The idle insertion and removal blocks are coupled to each other through the clock adaptation

block and its FIFO buffer 77. The adapted packets are transmitted then through output data ~~bocks~~ blocks 69. As will be understood from the description above, the functional blocks in Figure 4 can be built around the corresponding Figure 2 blocks to accomplish the same functions in reverse. As with the transmit path, there is a clock domain transition 76 and the FIFO buffer within the clock adaptation block is used to make the transition. In other applications, the positions and functions of the other modules 115 can be modified or distributed as appropriate.

Please delete the paragraph on page 20 beginning at line 1, under the header ABSTRACT, and replace with the following paragraph:

The present invention allows data transmissions to cross from one clock domain to another, in one embodiment, the invention includes an idle removing block operating at a first clock speed to remove idles ~~idle bits~~ from received data ~~packets~~ stream, a buffer coupled to the idle removing block to receive the data packets from the idle removing block, the buffer generating an idle ~~insertion~~ removal control signal to the idle removing block to enable the removal of idles ~~idle bits~~ by the idle removing block, and an idle insertion block coupled to the buffer to receive data ~~packets~~ stream from the buffer and insert idles ~~idle bits~~ into the data packets, the idle insertion block receiving an idle insertion control signal from the buffer to enable the insertion of idles ~~idle bits~~.

In the Claims:

1. (Amended) An apparatus comprising:

an idle removal block operating at a first clock speed to remove idles from received data packets;

a buffer coupled to the idle removal block to receive the data packets from the idle removal block, the buffer generating an idle ~~insertion~~ removal control signal to the idle removal block to enable the removal of idles by the idle removal block;

an idle insertion block operating at a second clock speed coupled to the buffer to receive data packets from the buffer and insert idles into the data packets, the idle insertion block ~~receiving~~ to receive an idle insertion control signal from the buffer to enable the insertion of idles.

2. (Amended) The apparatus of Claim 1 wherein the buffer comprises a dual port memory, wherein the idle removal block is coupled to one port of the dual port memory and wherein the idle ~~removal~~ insertion block is coupled to the other port of the dual port memory.

3. (Amended) The apparatus of Claim 1 wherein the buffer comprises write control logic for writing packets from the idle removal block into the buffer and wherein the write control logic generates the idle ~~insertion~~ removal control signal based on the write capacity of the buffer.

5. (Amended) The apparatus of Claim 1 wherein the buffer comprises read control logic for reading packets from the buffer and wherein the read control logic generates the idle insertion ~~removal~~ control signal based on the read capacity of the buffer.

8. (Amended) An apparatus comprising:

means, operating at a first clock speed, for removing idles from received data packets;

means for buffering data packets coupled to the means for removing for receiving the data packets from the means for removing, the means for buffering generating an idle ~~insertion~~ removal control signal to the means for removing to enable the removal of idles by the means for removing;

means, operating at a second clock speed, coupled to the means for buffering for receiving data packets from the means for buffering and for inserting idles into the data packets, the means for inserting receiving an idle insertion control signal from the means for buffering to enable the insertion of idles.

9. (Amended) The apparatus of Claim 8 wherein the means for buffering comprises a dual port memory, wherein the means for removing is coupled to one port of the dual port memory and wherein the means for ~~removing~~ inserting is coupled to the other port of the dual port memory.

10. (Amended) The apparatus of Claim 8 wherein the means for buffering comprises means for writing packets from the means for removing into the means for buffering and wherein the means for writing generates the idle removal ~~insertion~~ control signal based on the write capacity of the means for buffering.

12. (Amended) The apparatus of Claim 8 wherein the means for buffering comprises means for reading packets from the buffer and wherein the means for reading generates the idle ~~removal~~ insertion control signal based on the read capacity of the means for buffering.

17. (Amended) The method of Claim 15 further comprising inserting idles into the packet after reading the packet ~~to create a second packet~~ at the second clock rate.